IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JEFFREY JAY ANDERSON WALTER S. SCHOPFER MERLE L. MILLER	Group Art Unit:	2644
		Examiner:	W. F. BRINEY, III
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For:	METHOD AND APPARATUS FOR HANDLING VOICE AND DATA SIGNALS		

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
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Sir:

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8	
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Signature

On November 8, 2004, Appellants filed a Notice of Appeal in response to a Final Office Action dated July 12, 2004, issued in connection with the above-identified application. In support of their appeal, Appellants hereby submit an original and two copies of this Appeal Brief to the Board of Patent Appeals and Interferences in response to the Final Office Action dated July 12, 2004. The fee for filing this Appeal Brief is **$500.00**, the Commissioner is authorized to withdraw funds from **Legerity, Inc.'s** Deposit Account **No. 50-1591/TT3773.** In the event the monies in that account are insufficient, the Commissioner is authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2069.008300.

Also, a request for a 1-month extension of time to respond is included herewith. The fee for filing a one month extension is **$120.00**, the Commissioner is hereby authorized to withdraw funds from **Williams, Morgan & Amerson's P.C.** Deposit account **50-0786/2069.008300**. This 1-month extension will bring the due date to February 8, 2005.

No other fee is believed due as a result of the response contained herein. However, **should any fees under 37 C.F.R. §§ 1.16 to 1.21 (or any other section) be required for any reason, the Commissioner is authorized to deduct said fees from Legerity, Inc. Deposit Account No. 50-1591/TT3773/2069.008300.**

I. REAL PARTY IN INTEREST

The present application is owned by Legerity, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

The Examiner rejected claims 1-3, 8-10, 15-16, 19-21, and 24 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,477,249 (***Williamson***) in view of U.S. Patent No. 6,625,278 (***Hendricks***) and further in view of U.S. Patent No. 5,802,169 (***Frantz***). Claims 4-7, 11-14, 17-18, and 22-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over ***Williamson*** in view of ***Hendricks*** in view of ***Frantz*** and further in view of U.S. Patent No. 4,577,255 (***Martin***). The claims currently under consideration, *i.e.*, claims 1-24 are attached as Appendix A.

IV. STATUS OF AMENDMENTS

No amendments have been made since the Final Office Action.

V. SUMMARY OF THE INVENTION

Appellants' inventive methodologies are generally directed to associating time-based information with workpieces. Figure 1 illustrates a simplified block diagram of a communications system 5 in accordance with the present invention. The communications system 5 includes a line card 10 that interfaces with a telephonic device 12 over a subscriber line 20. The telephonic device 12 may comprise a telephone or any other device capable of providing a communication link between at least two users. A subscriber line interface circuit (SLIC) 30 is coupled to the subscriber line 20. Hereinafter, signals received by the line card 10 over the subscriber line 20 are referred to as upstream signals, and signals transmitted by the line card 10 on the subscriber line 20 are referred to as downstream signals.

The SLIC supplies an analog upstream signal to a coder/decoder (CODEC) 40. The CODEC 40 receives the analog upstream signal from the SLIC 30 and generates a digital upstream signal that is subsequently passed to a digital signal processor 50. The DSP 50 also provides a digital signal for eventual transmission on the subscriber line 20. The CODEC 40 receives the digital signal, converts it to an analog signal, and provides the analog signal to the SLIC 30, which sends the analog signal over the subscriber line 20.

In the illustrated embodiment, the line card 10, in addition to supporting plain old telephone service (POTS), is adapted to implement an asynchronous digital subscriber line

(ADSL) modem for high bandwidth data transfer. The SLIC 30 of the line card 10 is capable of performing a variety of functions, such as battery feed, overload protection, polarity reversal, on-hook transmission, and current limiting.

Figure 2 illustrates one embodiment of the line card 10 in accordance with the present invention. Specifically, the line card 10 includes the SLIC 30, which, in the illustrated embodiment, is a voltage-feed SLIC. The line card 10 also includes the CODEC/DSP 40, 50, which in the illustrated embodiment are shown as a subscriber line audio-process circuit (SLAC) 215 that integrates the functions of both the CODEC and DSP 40, 50. The line card 10 may be located at a central office or a remote location somewhere between the central office and the telephonic device 12 (see Figure 1). The line card 10 interfaces with the telephonic device 12 through tip and ring terminals 237, 239 at the SLIC 30. The combination of the telephone device 12 and the subscriber line 20 is generally referred to as a subscriber loop.

The standard impedance of the subscriber line 20 is herein denoted as Z_{LOOP}, and impedance seen by an incoming signal from the subscriber line 20 is hereinafter referred to as Z_{IN}. The value of Z_{LOOP}, which is determined by individual telephone authorities in various countries, may be in the range of 600-900 ohms for the POTS band and in the range of 100-135 ohms for the xDSL band. The SLIC 30 is adapted to be coupled to first and second (RFz) resistors 217, 219, which, as described below, are utilized to define the input impedance.

The line card 10, which may be capable of supporting a plurality of subscribers lines 20, performs, among other things, two fundamental functions: DC loop supervision and DC feed.

The purpose of DC feed is to supply enough power to the telephone device 12 at the customer end. The purpose of DC loop supervision is to detect changes in DC load, such as on-hook events, off-hook events and rotary dialing, or any other event that causes the DC load to change.

The voltage-feed SLIC 30 is a high voltage bipolar SLIC that drives voltages to the subscriber line 20 and senses current flow in the subscriber line 20. The SLIC 30 includes first and second differential line drivers 230, 235 that interface with the subscriber line 20 via tip and ring terminals 237, 239. The tip terminal 237 is coupled to a first terminal of a first sensing resistor (R_{ab}) 240 and to an inverting terminal of the first line driver 230. A second terminal of the first sensing resistor 240 is coupled to an output terminal of the first line driver 230. The ring terminal 239 is coupled to a first terminal of a second sensing resistor (R_{bd}) 245 and to an inverting terminal of the second line driver 235. A second terminal of the second sensing resistor 245 is coupled to an output terminal of the second line driver 235.

The SLIC 30 includes a sum block 250 and a current-sensing circuit 260. The sum block 250 includes a first output terminal coupled to a non-inverting terminal of the first line driver 230, and a second (inverted) output terminal coupled to a non-inverting terminal of the second line driver 235. The sum block 250 is capable of receiving a DC feed signal (as well as ringing signals) from a DCIN terminal 265, a voice signal, a metering signal, and a data signal and is capable of adding one or more of the received signals and providing it to the first and second line drivers 230, 235. The signals into the SUM block 250 may be subjected to different levels of gain for optimal performance. The signal from the DCIN terminal 265 is low-pass filtered.

The current-sensing circuit 260 produces a current proportional to the loop current through the current sensing resistors 240, 245, subtracts a current proportional to a current from a cancellation terminal (CANC) 270, and provides the resulting current to an IMT terminal 275 of the SLIC 30. Although not so limited, in the instant embodiment, the constant of proportionality (KCN) for the current from the cancellation terminal (CANC) 270 is unity, and the constant of proportionality for the metallic line current is 0.001.

The SLIC 30 includes a first impedance matching loop 262 that adjusts a nominal value of the input impedance (Z_{IN}) to substantially match the impedance of the subscriber line 20. The first impedance matching loop 262 includes a nominal Z block 263 that receives the output signal of the current sensing circuit and provides a selected amount of "fixed" gain and phase to adjust a nominal value of the input impedance, Z_{IN}. In the illustrated embodiment, the nominal Z block 263 sets the nominal value of the input impedance to a fixed value of 100 ohms plus 800 ohms in parallel with 34 nF, which includes the resistance provided by resistors 217, 219, 240 and 245.

The SLIC 30 is connected to the SLAC 215, an external resistor 280, as well as a capacitor 281. A first terminal of the resistor 280 is coupled to the IMT terminal 275 of the SLIC 30, as well as to the VIN terminal 285 of the SLAC 215. A second terminal of the resistor 280 is coupled to a reference voltage node 282, as well as to a terminal of the capacitor 281. In one embodiment, the reference voltage 282 is in the range of about 1.4 volts. The external resistor 280 and the capacitor 281 form a single-pole low pass filter 283 that is capable of filtering at least a portion, if not all, of the signals above the voice band, such as data signals and

metering signal. The external resistor 280 and the capacitor 281 convert the current flowing from the IMT terminal 275 to a proportional voltage signal for the SLAC 215.

A discrete network 288 couples the SLIC 30 to the SLAC 215 via the CANC terminals 270, 290. The discrete network 288 includes a first and second resistor 292, 294 and a capacitor 296. A first terminal of the first resistor 292 is coupled to the CANC terminal 270 of the SLIC 30 and a second terminal of the first resistor 292 is coupled to a first terminal of the second resistor 294. The second terminal of the second resistor 294 is coupled to the CANC terminal 290 of the SLAC 215. The capacitor 296 is coupled between the second terminal of the first resistor 292 and the reference voltage node 296. The discrete network 288 acts as a low pass filter and converts the voltage output signal from the SLAC 215 to a current and provides it to the SLIC 30.

The SLAC 215 interfaces with the telephonic device 12 through the SLIC 30 and over the subscriber line 20. The SLAC 215 includes two feedback loops: a DC cancellation loop 298 and a DC feed loop 300. In the illustrated embodiment, the two loops 298, 300 are implemented within a digital signal processor (DSP).

The DC cancellation loop 298 includes an analog-to-digital converter 305, DC cancellation logic 315, a current limiter 317, and a digital-to-analog converter 319. The analog-to-digital converter 305 and digital-to-analog converter 319 include a decimator and interpolator, respectively. The analog-to-digital converter 305 in the illustrated embodiment is capable of providing two output signals, the first output signal is sampled at a 4 KHz frequency and provided as a

digital signal to the DC cancellation logic 315, as well as to a switch hook detection logic 320. The second output signal of the analog-to-digital converter 305, comprising of voice and/or data (residual) components, is sampled at 32 KHz and provided to a CODEC (not shown). A residual data component may exist at the output of the analog-to-digital converter 305 since the single-pole low pass filter 283 may not remove all the data signal; however, this signal is removed by the decimator.

The DC cancellation logic 315 receives the digital signal from the analog-to-digital converter 305, filters high frequencies, and provides a substantially DC signal. The DC signal is provided as an input to the DC feed logic 321, as well as to the current limiter 317. The output of the current limiter 317 is converted to an analog signal and then provided back to the SLIC 30 via the CANC terminal 270. The output of the current limiter 317 is also provided to the switch hook detection logic 320 for switch hook detection during pulse dialing. The current provided to the CANC terminal 270 of the SLIC 30 is used to cancel the DC component of the signal from the current sense circuit 260. Thus, during a "stable" state (*i.e.*, no transients present), the signal at the VIN terminal 285 of the SLAC 215 is essentially DC free.

The DC feed loop 300, in addition to the analog-to-digital converter 305 and DC cancellation logic 315, includes DC feed logic 321 and a digital-to-analog converter 322. In the illustrated embodiment, the digital-to-analog converter 322 may also interpolate. The output from the digital-to-analog converter 322 is provided to a DCIN terminal 265 of the SLIC 30 via VHL terminal 323 of the SLAC 215. The DC feed logic 321 is capable of providing high DC voltage to the subscriber loop so that sufficient current (20-60 mA) can be driven through a

resistance as high as 2K ohms. When the DC conditions on the subscriber loop change suddenly, the DC feed logic 321 adapts to the change, thereby allowing normal transmission to continue. Examples of sudden changes in DC conditions include on-hook, off-hook, rotary dialing, and tone signaling. When the telephonic device 12 goes off-hook, the loop impedance drops almost instantly to a value below 2K ohms. In short subscriber loops, the loop impedance may be less than 200 ohms. For the line card 10 to function and transmit information properly, the DC conditions on the subscriber loop should be stabilized quickly, and in some cases, within milliseconds.

The SLAC 215 includes a second matching loop 324 that includes an impedance matching block 325. The impedance matching block 325 receives the signal from the VIN terminal 285 of the SLAC 215 and provides an output signal to an VOUT terminal 326 of the SLAC 215. The signal from the VOUT terminal 326 is provided to a VIN terminal 327 of the SLIC 30. The sum block 250 receives the signal from the VIN terminal 327 of the SLIC, sums the signal with other signals, such as DC feed signal, the data signal, and metering signal, and provides the resulting signal to the drivers 230, 235 of the SLIC 30.

When the line card is in a "stable" state (*i.e.*, no transients), the signal at the VIN terminal 285 of the SLAC 215 comprises primarily a voice signal, although it may include residual metering or data signals that are not removed by the single-pole low pass filter 283. This single-pole low pass filter 283 provides adequate performance by attenuating the data and metering signals to acceptable levels. Aside from being more cost effective than higher order low-pass

filters, the single-pole low pass filter 283 also provides an added advantage in that it is less likely to make the line card 10 unstable.

Referring now to Figure 4, a specific embodiment of the impedance matching module 325 is shown. As can be seen with reference to Figure 4, the impedance matching module 325 comprises three loops: an analog impedance scaling network (AISN) loop 350 and two Z-filter loops 355, 356. The AISN loop 350 includes an AISN block 358 that is coupled between the VIN and VOUT terminals 285, 326 of the SLAC 215. The signal present at the VIN terminal 285 of the SLAC 215 is low-pass filtered to prevent higher frequencies of the data band from impairing the function of the impedance matching module 325, although some frequencies above the voice band range that might not have been filtered may be present at the VIN terminal 285. The AISN block 358 may be a programmable impedance matching filter that is capable of varying the nominal value of the input impedance that is set by the nominal-Z block 263 (see Figure 2) of the SLIC 30. Typically, the AISN block 358 is effective in adjusting the input impedance for frequencies in the voice band. This impedance is relatively constant in the voice band.

The fixed analog gain forms an impedance which is equal to the product of the current sense gain (KIMT) times the impedance of the parallel combination of the external resistance (RIMT) and capacitance (CIMT) times the feedback (NOMINAL-Z) gain. Taking into account the external fuse resistance (RF), equation (1) below illustrates the impedance:

$$Z_{IN}^{(5)} = RFZ + KIMT * KZ * \frac{RIMT}{1 + RIMT * CIMT * S} \qquad (1)$$

where the exemplary values are as follows: RFZ = 100 Ω; KIMT = 0.001; NOMINAL-Z = 8; RIMT = 100 KΩ; and CIMT = 270 pF (+ 6 pF of stray capacitance). This leads to an input impedance of 100 Ω + (800 Ω || 35.5 F).

The programmable analog gain (AISN) inside the SLAC 215 has substantially the same effect as NOMINAL-Z. In the illustrated embodiment, the gain varies from -15/16 to +15/16 in 1/16 steps inside the SLAC 215. This is passed through a gain of KIN = 5 inside the SLIC 30. The effect is to increase or decrease KL by as much as 4.6875. This allows the 800 Ω resistor to be lowered to 331.25 Ω or raised to 1268.75 Ω. The corner frequency is unchanged.

The Z-filter loop 355 of the impedance matching module 325 receives a signal from the analog-to-digital converter 305. The analog-to-digital converter 305 converts the signal from the VIN terminal 285 of the SLAC 215 to a digital signal and delivers it to the high pass filter 370. In the illustrated embodiment, the analog-to-digital converter 305 also, through the process of decimation, reduces the frequency of the bits of the signal and provides a more accurate signal to the input terminals of the Z-filters 375, 376. The CANC input terminal 270 of the SLIC 30 is used to remove most of the DC feed component. The high-pass filter 370 substantially reduces the residual DC component, if one is present, from the received signal and provides primarily a voice-only-signal to an input terminal of the Z-filters 375, 376.

The Z-FIR filter 375 may be a programmable impedance matching filter that allows a user to program the gain factor, the phase shift, or a combination thereof to vary Z_{IN}. Typically, the Z-FIR filter 375 provides a frequency variable input impedance to the line card 10. The

Z-FIR filter 375 also attempts to account for delays in the input signal caused by digital processing, for example, during decimation and interpolation. The programmable Z-FIR filter 375 further modifies the analog gains with a frequency variable gain. This allows control of the midband frequency characteristics. For very high frequencies, the delay in the digital interpolation and decimators reduces the effectiveness of the Z-FIR filter 375. At low frequencies, the limited length of the Z-FIR filter limits the filter, and the Z-IIR filter 376 may then take over.

The Z-IIR filter 376 provides a single pole low pass filter for responses which demand a long exponential time response. This has the effect of applying what looks like a large capacitor in series with the rest of the network.

The output from the Z-FIR filter 375 and Z-IIR filter 376 is added and provided to a first signal adder 380, which adds the filter 375, 376 output to a downstream voice signal. The output of the first signal adder 380 is provided to a digital-to-analog converter 383 that converts the received signal and provides an analog output signal to a second signal adder 385. The second signal adds the signal from the AISN block 358 and the digital-to-analog converter 383 and provides a resulting signal to the VOUT terminal 326 of the SLAC 215. The signal from the VOUT terminal 326 of the SLAC 215 is delivered to the subscriber line 20 through the SLIC 30.

The input impedance, Z_{IN}, produced by the nominal Z block 263, AISN block 358, and Z-filters 375, 376 is calculated according to equation (2):

$$Z_{IN} = Kimt * R_{280} * (NOMINAL\text{-}Z + KIN*(Kaisn+Nominal\text{-}zfil))+R_{217}+R_{219}+R_{240}+R_{245} \quad (2)$$

where Kimt is the constant of proportionality for the metallic line current, R_{280}, R_{217}, R_{219}, R_{240}, and R_{245} correspond to the resistors shown in Figure 2 having respective values of 100000, 35, 35, 15, and 15 ohms, NOMINAL-Z is a fixed amount of injection gain in the SLIC 30 from IMT terminal 275 to the output of SLIC 30, KIN is a no-load gain from VIN terminal 327 of the SLIC to the output of the SLIC 30, Kaisn is an impedance adjustment factor of the AISN block 358, and Nominal-zfil is the frequency variable gain provided by the Z-filter 375.

For example, if a 600-ohm resistive impedance is required for the voice band, then the output of the AISN block 358 is adjusted so that Z_{IN} substantially equals 600 ohms. To obtain the desired 600 ohms resistive impedance, an exemplary value of Kaisn may be -0.6, as shown below. Furthermore, for illustrative purposes, assume that Kimt = 0.001, NOMINAL-Z = 8, and KIN = 5. Substituting the exemplary values provided above into equation (2) yields: Z_{IN} = 0.001 * 100000 * (8 + 5 * (-0.6 + 0)) + 35 + 35 + 15 + 15 = 600. There may be a capacitive element due to CIMT (281). This can be neutralized by a suitable choice of the digital Z-filter. Likewise, other values of resistive impedance may be obtained by adjusting the Kaisn and/or Nominal-zfil values.

The input impedance, Z_{IN}, for the data band is primarily governed by the values of resistors 217, 219, 240, and 235. This is because the low pass filter 283 between the IMT terminal 275 of the SLIC 30 and VIN terminal 285 of the SLAC 215, isolates the nominal Z block 263 (see Figure 2), AISN block 358, and Z-filter block 375 for the higher frequencies of the data band. When the data band is substantially isolated from the nominal Z block 263 and the impedance matching module 325, the natural impedance of the line card 10 substantially

equals the impedance of the data band. The data impedance is therefore set primarily by the resistors 217, 219, 240, and 245. Exemplary values of the resistors 217, 219, 240, and 245 are 35, 35, 15, and 15 ohms, respectively.

The method of Figures 5 can be implemented by the line card 10 of Figure 2 to adjust Z_{IN} to substantially match Z_{LOOP} for signals in the voice, as well as the data, band. The method of Figure 5 begins at block 710, where the line card 10 receives an input signal having at least one of a voice, data, and DC component. At block 720, the low-pass filter 283 filters at least a portion of the data component and DC component of the input signal to provide a filtered signal. At block 730, the nominal Z block 263 of the SLIC 30 adjusts the input impedance of the line card 10 to a first preselected value for the voice band in response to the filtered signal. For example, the nominal Z block 263 may adjust the input impedance of the line to 900 ohms, or to any other desirable level. An exact match is not required, as the AISN block 358 is utilized in accordance with the present invention to arrive at a more precise value.

At block 740, the AISN block 358 adjusts the input impedance of the first apparatus from the first preselected value to a second preselected value. Thus, for example, the second preselected value may be a more precise value of the first preselected value. In the illustrated embodiment, the AISN block 358 is implemented in an analog circuit in the SLAC 215. The AISN block 358 operates in combination with the nominal Z block 263 to arrive at or near the desired input impedance value. The AISN algorithm of the AISN block 358 includes a finite number of gain steps to arrive at the desired range of the input impedance. For this reason, it is desirable to utilize the nominal Z block 263 to first arrive in proximity to the first preselected

value of the input impedance and then use any of the remaining bits available to the AISN algorithm to obtain the second preselected value of the input impedance.

At block 750, the Z-filter block 375 adjusts the input impedance further in response to detecting at least one of attenuation and delay in the filtered signal. That is, the Z-filter block 375 is capable of modifying the gain and phase characteristics of the input signal by a selected amount to adjust Z_{IN} to substantially equal Z_{LOOP} for the POTS (*i.e.*, voice) band.

The AISN and Z-filter blocks 358, 375 may be implemented within a mixed signal integrated circuit. Furthermore, in accordance with the present invention, the two blocks may be implemented as hardware, software, or a combination thereof.

Of course, the present invention should not be considered as limited to the specifically disclosed embodiments discussed immediately above.

VI. ISSUES ON APPEAL

1. Whether claims 1-3, 8-10, 15-16, 19-21, and 24 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,477,249 (***Williamson***) in view of U.S. Patent No. 6,625,278 (***Hendricks***) and further in view of U.S. Patent No. 5,802,169 (***Frantz***)?
2. Claims 4-7, 11-14, 17-18, and 22-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over ***Williamson*** in view of ***Hendricks*** in view of ***Frantz*** and further in view of U.S. Patent No. 4,577,255 (***Martin***)?

VII. GROUPING OF THE CLAIMS

Claims 1-3, 8-10, 15-16, 19-21, and 24 are grouped together (Group I), and rise or fall together; claims 4-5, 7, 11-14, 17-18, and 22-23 are grouped together (Group II), and rise or fall together; and claim 6 is in its own group (Group III).

VIII. ARGUMENT

The Examiner relies on no less than three different references, and in many instances on four different references, to reject individual claims of the present patent application under §103 for obviousness. Despite the large number of references relied upon by the Examiner, these references, when considered alone or in combination, nevertheless fail to establish a *prima facie* case of obviousness.

The Federal Circuit has on numerous occasions outlined the requisite elements needed to establish a *prima facie* case of obviousness. In particular, the Federal Circuit has noted that at least the following showings must be made: (1) the prior art reference (or references when combined) must teach or suggest all the claim limitations; (2) there is some suggestion or motivation to modify the reference or to combine reference teachings; and (3) there is a reasonable expectation of success. As explained below, the Examiner here has failed to establish all three of these requisite elements.

Turning now to the present invention, in general, one or more embodiments of the present invention are directed to a multi-level impedance matching scheme. For example, in the illustrated embodiment, the nominal Z block 263 adjusts the input impedance to a first

preselected level, which represents a general range of the desired impedance level. Another block, namely the AISN block 358, further adjusts the input impedance level from the fist preselected level (determined by the Z block 263) to a second preselected level, which may be closer to the desired impedance level relative to the first preselected level. In an effort to arrive at the desired impedance level, the Z-filter block 375 may adjust at least one of a magnitude and phase of the filtered signal to adjust the input impedance to a third value. In this manner, the impedance level can be efficiently adjusted to the desired level. One or more of the claims are directed to one or more of these described features. The grouped claims are discussed next.

A. GROUP I CLAIMS ARE ALLOWABLE

1. THE CITED REFERENCES AT LEAST DO NOT TEACH A THREE-PRONG APPROACH FOR ADJUSTING THE INPUT IMPEDANCE

Claim 1 is directed to a method for impedance matching voice and data signals received by an apparatus. The method includes receiving an input signal having a voice, data, and DC component. Thus, according to this claim element, the "input signal" includes at least three different components: a voice component, data component, and DC component. The next element of claim 1 calls for filtering at least a portion of the data component and DC component of the input signal to provide a filtered signal. Thus, this element calls for removing at least a portion of the "data" and "DC" component of the input signal (which originally had at least 3 components) to provide a signal that mainly has a voice component (i.e., the filtered signal).

The next three elements of claim 1 call for at least a three-prong approach to adjusting the input impedance of the apparatus. The first step calls for adjusting the input impedance of the apparatus to a first preselected value for the voice band. The second step calls for adjusting the input impedance of the apparatus from the first preselected value to a second preselected value. And the third step calls for adjusting at least one of a magnitude and phase of the filtered signal to adjust the input impedance to a third value.

The Examiner argues that the first two elements of claim 19 are taught by Williamson and the third element is taught by Frantz. The remaining elements of claim 19, according to the Examiner, are taught by yet another reference, Hendricks. While the Examiner's asserts that Hendricks teaches the three-prong impedance-adjusting approach[1] of claim 1, a closer review of Hendricks reveals otherwise. As shown in Figure 1, Hendricks is directed to a telephone line interface circuit that includes a programmable digital filter 110 (sometimes called sigma delta filter) to "provide programmable AC impedance to a telephone line." *See* Hendricks, 2:46-48. Hendricks describes that the impedance matching is adjusted through the use of ZR block 170 and ZRX filter block 110. *See* Hendricks, col. 3, lines 53-55 (stating that impedance is matched through the parallel combination of ZRX and ZR). ZR, according to Hendricks, is a reference impedance that provides a partial solution to the AC impedance matching, and, as such, is called "helper impedance." *Id.* at col. 4, lines 4-7. ZRX, according to Hendricks, is the resultant AC impedance across points A and B of the telephone line that is adjusted by the signal delta filter 110 through the use of a current source 160. *Id.* at col. 4, lines 19-23; col. 4, lines 59-64.

[1] The pending claims are open ended claims, and thus are not limited to a three-prong impedance matching scheme; rather, the claims are intended to cover schemes with more than three prongs.

Hendricks makes clear that it is the sigma delta filter 110 that adjusts the impedance ZRX. Specifically, Hendricks describes that a gain or pole parameter of the sigma delta filter 110 can be adjusted, and that the adjustment of these parameters in turn controls the current source 160 to arrive at the desired ZRX impedance. *See* Hendricks, col. 4, lines 59-64 (stating "[i]n accordance with the principles of the present invention, the...sigma delta filter 110 has a programmable gain...and a programmable pole...[that] are used to affect the AC impedance to the telephone line, and therefore implement the AC impedance ZRX); *see also* col. 5, line 61 – col. 6, line 2. Thus, impedance matching in Hendricks occurs through the "helper impedance" provided by ZR block 170 and through ZRX adjustment made via the gain/pole of the filter 110.

According to the Examiner, element 170 (the ZR block) of Figure 1 of Hendricks adjusts the input impedance of the apparatus to a first preselected value for the voice band.[2] *See* page 3 of the Office Action, dated 5/12/2004. Next, the Examiner argues that element 160, which is a controlled current source, adjusts the input impedance of the apparatus from the first preselected value to a second preselected value." *Id.* The Examiner also contends that element 110 (ZRX) of Figure 1 of Hendricks adjusts at least one of a magnitude and phase of the filtered signal to adjust the input impedance to a third value." *Id.*

The Applicants respectfully disagree with the Examiner that Hendricks teaches [at least] a three-pronged arrangement for adjusting impedance in the manner claimed. As noted, the Examiner argues that current source 160 adjusts the input impedance of the apparatus from the

[2] While the Examiner specifically addresses claim 19 in the Final Office Action, the Examiner nevertheless argues that claim 1 (and other independent claims) are unpatentable over the cited references for the same reasons claim 19 is not patentable. Thus, the basis of Examiner's rejection of claim 19 appears to be the same for the other independent claims, including claim 1.

first preselected value to a second preselected value. The Examiner asserts that this claimed feature is described in Hendricks at col. 2, lines 19-40. *See* Final Office Action, page 3. This cited text describes that the sigma delta filter 110 controls the current source 160 to emulate an AC impedance in a given range, such as between 300 and 1050. The Examiner erroneously oversimplifies this description to suggest that it is only the current source 160 that emulates the AC impedance in the specified range. Rather, as explained above, Hendricks makes it clear that the AC impedance is adjusted by the filter 110, which in turn controls the current source 160 to arrive at the desired AC impedance. Specifically, the transfer function of the filter 110 is adjusted through the programmable gain/pole feature so that the current source 160 can be used to arrive at the desired range of 300 and 1050 ohms. *See* Hendricks, col. 4, lines 59-64

It is helpful to understand that it is the combination of the filter 110 and current source 160 that operates to achieve the desired impedance range in Hendricks because it highlights the flaw in the Examiner's argument. In Hendricks, there is no further impedance adjustment that is performed by the filter 110 that is separate and apart from the current source 160. In contrast, claim 1 calls for adjusting the input impedance to a third value. There is no such disclosure in Hendricks or any of the other applied references[1]. Indeed, the Examiner himself does not cite to any specific passage from Hendricks that discloses adjusting at least one of a magnitude and phase of the filtered signal to adjust the input impedance to a third value. Rather, to supposedly show this claimed feature, the Examiner resorts to generalities and cites to virtually the **entire** specification of Hendricks. *See* Final Office Action, page 4 (citing "column 2 -- column 5"). Because the applied references, including Hendricks, fail to teach each and every claimed

feature, claim 1 is allowable. For at least the same reason, the remaining claims in Group I are also allowable.

2. THERE IS NO REQUISITE SUGGESTION OR MOTIVATION TO COMBINE

As noted, the Examiner relies on a combination of the references Williamson, Hendricks, and Frantz to rejection Group I claims for obviousness. However, to establish a *prima facie* case of obviousness, the Federal Circuit has noted that there must be some suggestion or motivation to modify the reference or to combine reference teachings. Moreover, suggestion or motivation to combine two or more references cannot be supplied through abstraction but must be grounded in practical considerations flowing from "positive, concrete evidence of record which justifies a combination of primary and secondary references." *In re Regal*, 188 U.S.P.Q. (BNA)136, 139 (C.C.P.A. 1975) (n. 6). A simple assertion that such a combination would be obvious to one of ordinary skill in the art cannot substitute for the type of evidence required by *Regal*. *See Fine*, 5 U.S.P.Q.2d (BNA) at 1599-1600. Here, the Examiner has failed in his proof. In the instant case, the Examiner, prior to the filing of this appeal brief, has failed to provide even a single citation from any of the cited references that shows the requisite motivation to combine. Rather, the Examiner merely uses the claim language as a template to argue obviousness.

The Examiner's conclusory statements are grossly inadequate and thus do not meet the standard set forth by the Federal Circuit. For example, with respect to the combination of Frantz, the Examiner simply states "[i]t would have been obvious to one of ordinary skill in the art at the

[3] While Hendricks states that the "pole" and "gain" of the filter 110 can be adjusted, it also makes it clear that these parameters serve to adjust the ZRX input impedance in conjunction with the current source 160.

time of the invention to block DC signals from the impedance matching circuitry as taught by Frantz for the purposes of performing impedance matching only on AC signals input to the subscriber line interface circuit of Williamson in view of Hendricks." *See* Final Office Action, page 4.

A brief look at Williamson and Frantz reveals that not only is there no motivation to the combine the references in a manner suggested by the Examiner, but that these references, in fact, teach away from such combination. In the Final Office Action, the Examiner notes that Williamson fails to teach a second filter of claim 19 (*i.e.,* fails to teach filtering the DC component). *See* Final Office Action, page 4. To find the second filter, the Examiner turns to Frantz, and argues that it discloses a capacitor 115 (see Figure 1) that blocks DC components and allows voice-band signals to pass through. *Id.*

As shown in Figure 1, Frantz discloses inserting a capacitor 115 at the tip and ring terminals of a telephone line to block DC components. Frantz describes that the capacitor 115 thus blocks DC signals and "allows only the voice-band signals to pass to...transformer 14." *See* Frantz, col. 3, lines 55-60. From the transformer 14, the voice-band signals are passed to the rest of the circuit for processing.

Williamson teaches a low pass filter (LPF) that handles speech traffic and signaling traffic of POTS signals. *See* Williamson, col. 3, lines 1-15; col. 3, lines 39-51, col. 4, lines 17-28; col. 4, lines 29-45; col. 4, lines 46-57. Specifically, Williamson describes a splitter that includes a low-pass filter where the filter's response time is varied depending on whether the

incoming telephony signal comprises speech traffic or signaling traffic. *Id.* The low pass filters used for speech and signaling are shown in Figures 9A and 9B of Williamson. As can been seen in Figures 9A and B, these low pass filters include an inductor in combination with capacitors (C1 and C2). Williamson describes that the "**main requirements**" of the LPF include passing the "DC line voltage of up to 100V without breakdown" and further taking "a DC current of 50 mA without saturation); *see also* col. 5, lines 25-31. Thus, while Williamson expressly says that the "main requirements" of the LPF are to pass DC line voltage or to take DC current, the Examiner's purposed combination of Frantz with Williamson would completely undermine this stated requirement. That is, if the DC-blocking capacitor of Frantz is inserted at the input of the telephone line in Williamson (much like it is in Frantz), the DC blocking-capacitor would prevent the low pass filters of Williamson from achieving their "main requirements." Thus, not only is there no requisite motivation to combine here (as evidenced by Examiner's conclusory statements), these references, in fact, teach away from the combination proposed by the Examiner.

The Examiner also fails to establish the requisite motivation to combine with respect to the Hendricks reference. Again, the Examiner makes general, unsubstantiated statements that are woefully inadequate to satisfy the criteria set forth by the Federal Circuit to show the requisite suggestion or motivation to combine. For example, the Examiner states "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to use the impedance matching filter of Hendricks with a first loop for the purpose of matching the terminating impedance of the subscriber line card of Williamson to the impedance of the

subscriber line with increased flexibility over the switchable filter arrangement of Williamson." This statement fails to establish a *prima facie* case of obviousness.

3. THERE IS NO REASONABLE EXPECTATION OF SUCCESS

The third requirement to establish a *prima facie* case of obviousness is reasonable expectation of success. Here, even assuming *arguendo* that the cited references were properly combinable (and they are not) and that they teach all of the claimed features (which they do not), the Examiner has nevertheless failed to establish that such a combination would have a reasonable expectation of success. Thus, for this additional reason, Group I claims are allowable.

B. GROUP III CLAIM IS ALLOWABLE

Claim 6 indirectly depends from claim 1, and thus is allowable for at least the reasons specified above with respect to Group I claims. Claim 6 is allowable for an additional reason in that it calls for a claimed feature not disclosed in the applied references. Claim 6 calls for "adjusting the frequency characteristic of the filtered signal by a selected interval." The Examiner argues that this feature is taught by Hendricks. However, Hendricks has no such teaching or disclosure, and, not surprisingly, the Examiner does not cite to any specific text in support of this rejection. Rather, the Examiner merely alleges, without providing any specific citation, that this feature is taught by Hendricks. Because neither Hendricks nor any of the other applied references teach this claimed feature, claim 6 is allowable.

Moreover, claim 6 is further allowable because the Examiner has failed to provide the requisite motivation to combine FOUR references (Williamson, Hendricks, Frantz, and Martin) in the manner suggested by the Examiner. Like in the other instances, the Examiner again makes conclusory statements that "it would have been obvious" to modify the teachings of said references. As stated, this is an inadequate showing to prove requisite motivation to combine. Accordingly, for this additional reason, claim 6 is allowable.

Additionally, the Examiner has failed to prove a reasonable expectation of success in view of the suggested combination. Accordingly, claim 6 is allowable for this further reason.

C. GROUP II CLAIMS ARE ALLOWABLE

In rejecting Group II claims, the Examiner adds yet another reference, Martin, thus bringing the total number of references to FOUR. The Group II claims directly or indirectly depend from Group I claims. Thus, Group II claims are allowable for at least the reasons Group I claims are allowable.

In combining the teachings of Martin, the Examiner once again relies on conclusory statements, thus failing to adequately show the requisite motivation or teaching to combine. Likewise, the Examiner fails to show a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20

U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. In the instant case, the Examiner has also failed to identify the requisite motivation to combine and expectation of success.

Thus, for at least these additional reasons, Group II claims are allowable.

IX. CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims pending in the present application, claims 1-24, over the prior art of record. The undersigned Ruben S. Bains may be contacted at (713) 934-4064 with respect to any questions, comments, or suggestions relating to this appeal.

Respectfully submitted,

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IN THE CLAIMS

1. (Original) A method of impedance matching voice and data signals received by an apparatus, comprising:

receiving an input signal having at least one of a voice component, data component, and DC component;

filtering at least a portion of the data component and DC component of the input signal to provide a filtered signal;

adjusting an input impedance of the apparatus to a first preselected value for the voice band in response to the filtered signal;

adjusting the input impedance of the apparatus from the first preselected value to a second preselected value; and

adjusting at least one of a magnitude and phase of the filtered signal to adjust the input impedance to a third value.

2. (Original) The method of claim 1, wherein filtering at least the portion of the DC component includes filtering the DC component using a DC cancellation loop.

3. (Original) The method of claim 1, wherein filtering at least a portion of the data component includes filtering at least portion of the data component using a single-pole low pass filter.

4. (Original) The method of claim 1, further including adjusting the input impedance of the apparatus to a fourth preselected value for the data band.

5. (Original) The method of claim 4, wherein the fourth preselected value is in a range of 100 to 135 ohms.

6. (Original) The method of claim 4, wherein adjusting the input impedance includes adjusting the frequency characteristic of the filtered signal by a selected interval.

7. (Original) The method of claim 4, wherein the first preselected value is in a range of 600 to 1200 ohms.

8. (Original) An apparatus for impedance matching, comprising:

circuitry adapted to receive an input signal having at least one of a voice, data, and DC component;

a first filter adapted to filter at least a portion of the data component of the input signal to provide a filtered data signal;

a second filter adapted to filter at least a portion of the DC component of the filtered data signal to provide a filtered signal;

a first impedance block adapted to adjust an input impedance of the apparatus to a first preselected value for the voice band in response to the filtered signal;

a second impedance block adapted to adjust the input impedance of the apparatus from the first preselected value to a second preselected value; and

a third impedance block adapted to adjust at least one of a magnitude and phase of the filtered signal to adjust the input impedance to a third value.

9. (Original) The apparatus of claim 8, wherein the second filter includes a DC cancellation loop capable of removing the portion of the DC component.

10. (Original) The apparatus of claim 8, wherein the first filter comprises a single-pole low pass filter.

11. (Original) The apparatus of claim 8, further including at least one resister for defining the input impedance of the apparatus to a fourth preselected value for the data band.

12. (Original) The apparatus of claim 11, wherein the fourth preselected value is in a range of 100 to 135 ohms.

13. (Original) The apparatus of claim 12, wherein the second impedance block and the third impedance block comprise a programmable impedance matching filter.

14. (Original) The apparatus of claim 12, wherein the first impedance block adapted to adjust the input impedance includes the first impedance block adapted to adjust the frequency of the filtered signal.

15. (Original) An apparatus for impedance matching, comprising:

circuitry adapted to receive an input signal having a voice, data, and DC component;

a first filter adapted to filter at least a portion of the data component of the input signal to provide a filtered data signal;

a second filter adapted to filter at least a portion of the DC component of the filtered data signal to provide a filtered signal;

a first feedback loop adapted to adjust an input impedance of the apparatus to a first preselected value for the voice band in response to the filtered signal;

a second feedback loop adapted to adjust the input impedance of the first apparatus from the first preselected value to a second preselected value; and

a third feedback loop adapted to adjust at least one of a magnitude and phase of the filtered signal to adjust the input impedance to a third value.

16. (Original) The apparatus of claim 15, wherein the third feedback loop comprises:

a filter capable of removing at least a portion of a residual DC component from the filtered signal and providing an output signal; and

a Z-filter block capable of adjusting a frequency response of the output signal.

17. (Original) The apparatus of claim 15, further including at least one resister for defining the input impedance of the apparatus to a fourth preselected value for the data band.

18. (Original) The apparatus of claim 17, wherein the fourth preselected value is in a range of 100 to 135 ohms.

19. (Original) An apparatus supporting transmission of signals carrying voice and data on a subscriber line, comprising:

a subscriber line interface circuit adapted receive an input signal having a voice, data, and DC component;

a first filter adapted to filter at least a portion of the data component of the input signal to provide a filtered data signal;

a second filter adapted to filter at least a portion of the DC component of the filtered data signal to provide a filtered signal; and

wherein the subscriber line interface circuit includes a first loop adapted adjust an input impedance of the apparatus to a first preselected value for the voice band in response to the filtered signal; and

a digital signal processor comprising:

a second feedback loop adapted to adjust the input impedance of the apparatus from the first preselected value to a second preselected value; and

a third feedback loop adapted to adjust at least one of a magnitude and phase of the filtered signal to adjust the input impedance to a third value.

20. (Original) The apparatus of claim 19, wherein the subscriber line integrated circuit is a voltage subscriber line interface circuit.

21. (Original) The apparatus of claim 19, the third feedback loop comprises:

a filter capable of removing at least a portion of a residual DC component from the filtered signal and providing an output signal; and

a Z-filter block capable of adjusting at least one of a gain and phase of the output signal.

22. (Original) The apparatus of claim 21, further including at least one resister for defining the input impedance of the apparatus to a selected value for the data band.

23. (Original) The apparatus of claim 22, wherein the selected value is in a range of 100 to 135 ohms.

24. (Original) An apparatus, comprising:

means for receiving an input signal having at least one of a voice component, data component, and DC component;

means for filtering at least a portion of the data component and DC component of the input signal to provide a filtered signal;

means for adjusting an input impedance of the apparatus to a first preselected value for the voice band in response to the filtered signal;

means for adjusting the input impedance of the first apparatus from the first preselected value to a second preselected value; and

means for adjusting at least one of a magnitude and phase of the filtered signal to adjust the input impedance to a third value.